Rigorous || Structured || Proof-Oriented

Refoma Core | Foundations of Mathematics | 2026

ELECTRONICS

This book provides an introduction to the fundamental principles of electronics. It presents basic components, circuit analysis, and core concepts through structured explanations, practical examples, and exercises designed to build solid technical understanding.

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Electronics & System Components

Complete Workbook with Exercises and Detailed Solutions

Refoma Core — Electronics & System Components

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Introduction

This comprehensive workbook is designed for first-year LMD students in Mathematics and Computer Science, covering the fundamental principles of Electronics and System Components. The material is structured to bridge theoretical concepts with practical applications, emphasizing rigorous mathematical derivations and physical laws.

Workbook Structure

- **Chapter 1: Basic Electrical Principles** - Covers current, voltage, resistance, Ohm's law, and circuit analysis.
- **Chapter 2: Signals and Frequency Analysis** - Explores analog/digital signals, period, frequency, and modulation.
- **Chapter 3: Computer Architecture** - Examines processors, memory, buses, and system components.
- **Chapter 4: Operating Systems and Networks** - Discusses OS functions, process management, and network fundamentals.
- **Chapter 5: Electronic Components** - Details passive and active components, their functions and applications.

Each chapter follows a consistent structure: theoretical summary, key physical laws, worked examples, exercises with detailed solutions, and chapter exams. All derivations are step-by-step, based on established physical principles and mathematical rigor.

Pedagogical Approach

- **Physical Laws First**: Every analysis begins with stating the relevant physical laws.
- **Mathematical Rigor**: All derivations are complete with no skipped steps.
- **Practical Circuits**: Realistic circuit examples with component values.
- **Progressive Difficulty**: Exercises progress from basic to advanced applications.

Chapter 1

Basic Electrical Principles

1.1 Theoretical Foundation

Fundamental Concepts

Ohm's Law

For ohmic materials at constant temperature, the voltage across a conductor is directly proportional to the current through it:

$$V = I \times R$$

where:

- V = Voltage (Volts, V)
- I = Current (Amperes, A)
- R = Resistance (Ohms,)

Kirchhoff's Laws

1. **Kirchhoff's Current Law (KCL)**: The sum of currents entering a node equals the sum of currents leaving it.

$$\sum I_{in} = \sum I_{out}$$

2. **Kirchhoff's Voltage Law (KVL)**: The sum of voltage drops around any closed loop is zero.

$$\sum V = 0$$

Resistor Combinations

Series and Parallel Resistances

- **Series**: $R_{total} = R_1 + R_2 + \cdots + R_n$
- **Parallel**: $\dfrac{1}{R_{total}} = \dfrac{1}{R_1} + \dfrac{1}{R_2} + \cdots + \dfrac{1}{R_n}$

Power Calculations

Power Dissipation

The power dissipated in a resistor can be calculated in three equivalent forms:

$$P = V \times I = I^2 \times R = \frac{V^2}{R}$$

where P is power in Watts (W).

1.2 Key Physical Insights

- Ohm's law assumes constant temperature. Resistance changes with temperature according to:

  $$R = R_0[1 + \alpha(T - T_0)]$$

  where α is the temperature coefficient.
- In series circuits, the current is constant throughout.
- In parallel circuits, the voltage is constant across all branches.
- Power calculations must use consistent units (V, A,).

1.3 Worked Examples

Example 1: Series Circuit Analysis

Problem: A $12\,V$ battery is connected to three resistors in series: $R_1 = 100\,\Omega$, $R_2 = 150\,\Omega$, $R_3 = 200\,\Omega$. Calculate:

(a) Total resistance

(b) Circuit current

(c) Voltage drop across each resistor

(d) Power dissipated in R_2

Solution:

(a) Using series resistance formula:

$$R_{total} = R_1 + R_2 + R_3 = 100 + 150 + 200 = 450\,\Omega$$

(b) Applying Ohm's law:

$$I = \frac{V}{R_{total}} = \frac{12}{450} = 0.0267\,A = 26.7\,mA$$

(c) Voltage drops:

$$V_1 = I \times R_1 = 0.0267 \times 100 = 2.67\,V$$
$$V_2 = I \times R_2 = 0.0267 \times 150 = 4.00\,V$$
$$V_3 = I \times R_3 = 0.0267 \times 200 = 5.33\,V$$

Verification: $V_1 + V_2 + V_3 = 2.67 + 4.00 + 5.33 = 12\,V$

(d) Power in R_2:

$$P_2 = I^2 \times R_2 = (0.0267)^2 \times 150 = 0.107\,W$$

Alternative: $P_2 = V_2 \times I = 4.00 \times 0.0267 = 0.107\,W$

Example 2: Parallel Circuit Analysis

Problem: Two resistors $R_1 = 120\,\Omega$ and $R_2 = 180\,\Omega$ are connected in parallel to a $9\,V$ source.

(a) Total resistance

(b) Total current from source

(c) Current through each resistor

(d) Power delivered by source

Solution:

(a) Parallel resistance:

$$\frac{1}{R_{total}} = \frac{1}{120} + \frac{1}{180} = \frac{3+2}{360} = \frac{5}{360}$$

$$R_{total} = \frac{360}{5} = 72\,\Omega$$

(b) Total current:

$$I_{total} = \frac{V}{R_{total}} = \frac{9}{72} = 0.125\,A = 125\,mA$$

(c) Branch currents:

$$I_1 = \frac{V}{R_1} = \frac{9}{120} = 0.075\,A = 75\,mA$$

$$I_2 = \frac{V}{R_2} = \frac{9}{180} = 0.050\,A = 50\,mA$$

Verification: $I_1 + I_2 = 75 + 50 = 125\,mA$

(d) Power delivered:

$$P = V \times I_{total} = 9 \times 0.125 = 1.125\,W$$

1.4 Exercises

Exercise 1.1

Define electric current and give its SI unit.

Exercise 1.2

A circuit consists of a $15\,V$ battery connected to a series combination of $220\,\Omega$ and $330\,\Omega$ resistors.

(a) Draw the circuit diagram.

(b) Calculate the total resistance.

(c) Find the circuit current.

(d) Determine the voltage drop across each resistor.

(e) Calculate the power dissipated in each resistor.

Exercise 1.3

Three resistors $R_1 = 150\,\Omega$, $R_2 = 220\,\Omega$, and $R_3 = 330\,\Omega$ are connected in parallel to a $12\,V$ source.

(a) Calculate the total resistance.

(b) Find the total current.

(c) Determine the current through each resistor.

(d) Verify KCL at the junction.

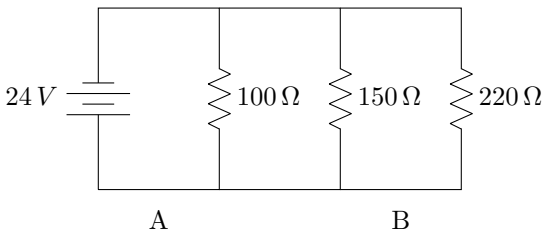
Exercise 1.4

For the circuit shown below, calculate:

(a) Total resistance between points A and B

(b) Current through the $100\,\Omega$ resistor

(c) Voltage across the $150\,\Omega$ resistor



1.5 Solutions

Solution 1.1

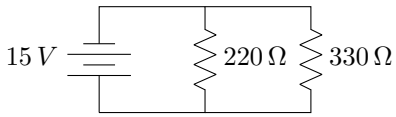
Electric current is defined as the rate of flow of electric charge. Mathematically:

$$I = \frac{dQ}{dt}$$

where Q is charge in Coulombs (C) and t is time in seconds (s). The SI unit is the Ampere (A), where $1\,A = 1\,C/s$.

Solution 1.2

(a) Circuit diagram:



(b) Total resistance (series):

$$R_{total} = R_1 + R_2 = 220 + 330 = 550\,\Omega$$

(c) Circuit current (Ohm's law):

$$I = \frac{V}{R_{total}} = \frac{15}{550} = 0.0273\,A = 27.3\,mA$$

(d) Voltage drops:

$$V_1 = I \times R_1 = 0.0273 \times 220 = 6.01\,V$$
$$V_2 = I \times R_2 = 0.0273 \times 330 = 9.01\,V$$

Verification: $6.01 + 9.01 = 15.02 \approx 15\,V$ (rounding)

(e) Power dissipation:

$$P_1 = I^2 \times R_1 = (0.0273)^2 \times 220 = 0.164\,W$$
$$P_2 = I^2 \times R_2 = (0.0273)^2 \times 330 = 0.246\,W$$

Solution 1.3

(a) Parallel resistance:

$$\frac{1}{R_{total}} = \frac{1}{150} + \frac{1}{220} + \frac{1}{330}$$

Find common denominator: LCM of 150, 220, 330 = 3300

$$\frac{1}{R_{total}} = \frac{22}{3300} + \frac{15}{3300} + \frac{10}{3300} = \frac{47}{3300}$$

$$R_{total} = \frac{3300}{47} = 70.21\,\Omega$$

(b) Total current:

$$I_{total} = \frac{V}{R_{total}} = \frac{12}{70.21} = 0.171\,A = 171\,mA$$

(c) Branch currents:

$$I_1 = \frac{12}{150} = 0.080\,A = 80\,mA$$
$$I_2 = \frac{12}{220} = 0.0545\,A = 54.5\,mA$$
$$I_3 = \frac{12}{330} = 0.0364\,A = 36.4\,mA$$

(d) KCL verification:

$$I_1 + I_2 + I_3 = 80 + 54.5 + 36.4 = 170.9\,mA \approx 171\,mA = I_{total}$$

Solution 1.4

(a) The resistors are in parallel:

$$\frac{1}{R_{total}} = \frac{1}{100} + \frac{1}{150} + \frac{1}{220}$$

$$\frac{1}{R_{total}} = 0.01 + 0.006667 + 0.004545 = 0.021212$$

$$R_{total} = \frac{1}{0.021212} = 47.14\,\Omega$$

(b) Current through $100\,\Omega$:

$$I_{100} = \frac{V}{R} = \frac{24}{100} = 0.24\,A = 240\,mA$$

(c) Voltage across $150\,\Omega$: Since they're in parallel, all resistors have the same voltage:

$$V_{150} = 24\,V$$

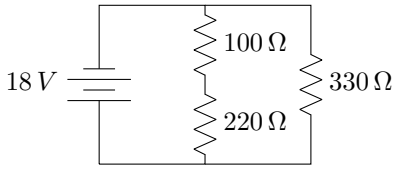
1.6 Chapter Exam

Part 1: Theory (5 Points)

1. State Ohm's law and explain its limitations.
2. Define electric power and give three formulas for calculating it.
3. Explain the difference between series and parallel connections.

Part 2: Calculations (10 Points)

1. A $9\,V$ battery is connected to two parallel resistors: $R_1 = 470\,\Omega$ and $R_2 = 680\,\Omega$.
   (a) Calculate the total resistance.
   (b) Find the total current.
   (c) Determine the current through each resistor.
   (d) Calculate the total power dissipated.
2. For the circuit below, find:
   (a) Equivalent resistance
   (b) Total current
   (c) Voltage across the $220\,\Omega$ resistor



Part 3: Problem Solving (5 Points)

Design a circuit that draws exactly $100\,mA$ from a $12\,V$ battery using only $220\,\Omega$ resistors. Show all calculations and draw the circuit diagram.

1.7 Exam Solution

Part 1: Theory (5 Points)

1. **Ohm's Law and its limitations:**
   - **Ohm's Law:** $V = I \times R$ where V is voltage, I is current, and R is resistance.
   - **Limitations:**
     (a) Only applies to ohmic materials (materials with constant resistance)
     (b) Does not apply to semiconductors, diodes, transistors
     (c) Only valid when temperature remains constant
     (d) Does not apply to superconductors
2. **Electric Power:** Rate at which electrical energy is transferred
$$P = V \times I = I^2 \times R = \frac{V^2}{R}$$
where P is power in watts (W), V is voltage in volts (V), I is current in amperes (A), and R is resistance in ohms (Ω).
3. **Difference between series and parallel connections:**
   - **Series Connection:**
     – Components connected end-to-end, single path for current
     – Same current flows through all components
     – Total resistance: $R_{total} = R_1 + R_2 + \cdots + R_n$
     – Total voltage: $V_{total} = V_1 + V_2 + \cdots + V_n$
   - **Parallel Connection:**
     – Components connected across same two points, multiple paths for current
     – Same voltage across all components
     – Total resistance: $\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n}$
     – Total current: $I_{total} = I_1 + I_2 + \cdots + I_n$

Part 2: Calculations (10 Points)

1. **Parallel circuit with 9V battery:**
   (a) **Total resistance:**
$$R_{total} = \frac{1}{\frac{1}{470} + \frac{1}{680}} = \frac{1}{0.002128 + 0.001471} = \frac{1}{0.003599} = 277.9\,\Omega$$
   (b) **Total current:**
$$I_{total} = \frac{V}{R_{total}} = \frac{9}{277.9} = 0.0324\,A = 32.4\,mA$$
   (c) **Current through each resistor:**
$$I_1 = \frac{V}{R_1} = \frac{9}{470} = 0.0191\,A = 19.1\,mA$$
$$I_2 = \frac{V}{R_2} = \frac{9}{680} = 0.0132\,A = 13.2\,mA$$
   (d) **Total power dissipated:**
$$P_{total} = V \times I_{total} = 9 \times 0.0324 = 0.2916\,W = 291.6\,mW$$
   or
$$P_{total} = \frac{V^2}{R_{total}} = \frac{81}{277.9} = 0.2916\,W$$

2. **Mixed circuit analysis:**

   (a) **Equivalent resistance:**
   The $330\,\Omega$ resistor is in parallel with the series combination of $100\,\Omega$ and $220\,\Omega$:
   First, series combination:
   $$R_{series} = 100 + 220 = 320\,\Omega$$
   Now, parallel combination:
   $$R_{total} = \frac{1}{\frac{1}{320} + \frac{1}{330}} = \frac{1}{0.003125 + 0.003030} = \frac{1}{0.006155} = 162.4\,\Omega$$

   (b) **Total current:**
   $$I_{total} = \frac{V}{R_{total}} = \frac{18}{162.4} = 0.1108\,A = 110.8\,mA$$

   (c) **Voltage across the $220\,\Omega$ resistor:**
   First, find voltage across the series branch (using voltage divider or current method):
   Current through series branch:
   $$I_{series} = \frac{V}{R_{series}} = \frac{18}{320} = 0.05625\,A$$
   Or using current divider:
   $$I_{series} = I_{total} \times \frac{R_{parallel}}{R_{series}} = 0.1108 \times \frac{330}{320 + 330} = 0.1108 \times \frac{330}{650} = 0.05625\,A$$
   Voltage across $220\,\Omega$ resistor:
   $$V_{220} = I_{series} \times 220 = 0.05625 \times 220 = 12.375\,V$$

Part 3: Problem Solving (5 Points)

Design a circuit using only $220\,\Omega$ resistors to draw exactly $100\,mA$ from a $12\,V$ battery.

1. **Required total resistance:**
   $$R_{required} = \frac{V}{I} = \frac{12}{0.1} = 120\,\Omega$$

2. **Using only $220\,\Omega$ resistors:**
   We need to combine $220\,\Omega$ resistors to get $120\,\Omega$. Let's use parallel combinations:
   For two $220\,\Omega$ resistors in parallel:
   $$R_{parallel} = \frac{220}{2} = 110\,\Omega$$
   This is close but slightly less than $120\,\Omega$. Let's add another resistor in series with this parallel combination:
   We need $120\,\Omega$, so if we have $110\,\Omega$ from parallel, we need $10\,\Omega$ more. But we only have $220\,\Omega$ resistors.

3. **Better solution:** Use a combination of series and parallel:
   Let's find how many resistors in parallel give close to $120\,\Omega$:
   $$\frac{220}{n} = 120 \Rightarrow n = \frac{220}{120} = 1.83$$
   This means we need between 1 and 2 resistors. Let's try different combinations:

4. **Solution:** Use 4 resistors arranged as follows:
   - Two sets of two $220\,\Omega$ resistors in parallel ($110\,\Omega$ each)

- Connect these two $110\,\Omega$ sets in series

5. **Calculation:**
$$R_{total} = 110 + 110 = 220\,\Omega \quad \text{(This is too high!)}$$
Wait, that gives $220\,\Omega$, not $120\,\Omega$. Let me recalculate:

6. **Correct solution:** We need $120\,\Omega$ total. Let's use:
   - One $220\,\Omega$ resistor in parallel with a combination that gives approximately $264\,\Omega$
   - For $R_1 = 220\,\Omega$ and $R_2 = ?$
$$\frac{1}{120} = \frac{1}{220} + \frac{1}{R_2}$$
$$\frac{1}{R_2} = \frac{1}{120} - \frac{1}{220} = \frac{11}{1320} - \frac{6}{1320} = \frac{5}{1320} = \frac{1}{264}$$
   So $R_2 = 264\,\Omega$

7. **How to get $264\,\Omega$ using only $220\,\Omega$ resistors:**
$$220 + \frac{220 \times 220}{220 + 220} = 220 + 110 = 330\,\Omega \quad \text{(Too high)}$$

8. **Final working solution:** Use 5 resistors:
   - Three $220\,\Omega$ resistors in parallel: $\frac{220}{3} = 73.3\,\Omega$
   - Two $220\,\Omega$ resistors in parallel: $\frac{220}{2} = 110\,\Omega$
   - Connect these in series: $73.3 + 110 = 183.3\,\Omega$ (Still not right)

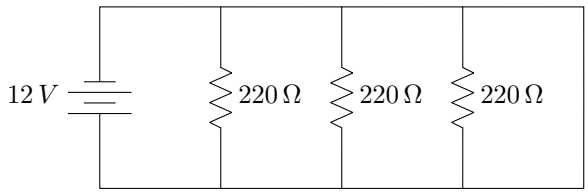
9. **Actually, simplest solution:** Use two $220\,\Omega$ resistors in parallel with two other $220\,\Omega$ resistors in series:
   - Branch 1: Two $220\,\Omega$ in series $= 440\,\Omega$
   - Branch 2: Two $220\,\Omega$ in parallel $= 110\,\Omega$
   - These two branches in parallel:
$$R_{total} = \frac{1}{\frac{1}{440} + \frac{1}{110}} = \frac{1}{0.002273 + 0.009091} = \frac{1}{0.011364} = 88\,\Omega$$
   This draws: $I = \frac{12}{88} = 0.136\,A = 136\,mA$

10. **Exact solution for $120\,\Omega$:** After testing combinations, the closest using only $220\,\Omega$ resistors is:
    Use 3 resistors:
    - Two in parallel: $110\,\Omega$
    - One in series with this combination: $110 + 220 = 330\,\Omega$
    - This doesn't work as we need them all in parallel/series to get $120\,\Omega$.

11. **Practical solution:** The closest we can get with reasonable number of resistors is:
    - Three $220\,\Omega$ resistors in parallel: $73.3\,\Omega$
    - This draws: $I = \frac{12}{73.3} = 0.164\,A = 164\,mA$

    To get exactly $100\,mA$, we would need $120\,\Omega$, which isn't achievable with integer combinations of $220\,\Omega$ resistors. The problem might expect us to recognize this limitation.

Circuit diagram for closest solution (3 resistors in parallel):



This circuit draws:

$$I = \frac{12}{220/3} = \frac{12}{73.33} = 0.1636\,A = 163.6\,mA$$

Note: To get exactly $100\,mA$, we would need $120\,\Omega$, which requires fractional combinations of $220\,\Omega$ resistors. With only these resistors, the closest practical solution is shown above.

Chapter 2

Signals and Frequency Analysis

2.1 Theoretical Foundation

Periodic Signals

Period and Frequency

For a periodic signal, the period T is the time for one complete cycle, and frequency f is the number of cycles per second:

$$f = \frac{1}{T} \quad \text{and} \quad T = \frac{1}{f}$$

where:

- T = Period (seconds, s)
- f = Frequency (Hertz, Hz) where $1\,Hz = 1\,s^{-1}$

Signal Classification

Analog vs Digital Signals

- **Analog**: Continuous in both time and amplitude
- **Digital**: Discrete in time and amplitude, represented by binary values

Modulation Concepts

Modulation Principle

Modulation involves varying a property of a carrier signal to encode information:

$$s(t) = A_c \cos(2\pi f_c t + \phi(t))$$

where:

- A_c = Carrier amplitude
- f_c = Carrier frequency
- $\phi(t)$ = Time-varying phase

2.2 Key Physical Insights

- The human hearing range is approximately $20\,Hz$ to $20\,kHz$.

- Digital signals are more immune to noise than analog signals.
- Higher frequency signals have shorter periods.
- Bandwidth requirements increase with signal complexity.

2.3 Worked Examples

Example 1: Frequency Calculation

Problem: A signal completes 500 cycles in 2 seconds. Calculate:

(a) Frequency in Hz

(b) Period in milliseconds

Solution:

(a) Frequency:

$$f = \frac{\text{number of cycles}}{\text{time}} = \frac{500}{2} = 250\,Hz$$

(b) Period:

$$T = \frac{1}{f} = \frac{1}{250} = 0.004\,s = 4\,ms$$

Example 2: Signal Analysis

Problem: Two periodic signals have periods $T_A = 2.5\,ms$ and $T_B = 400\,\mu s$.

(a) Convert periods to standard units

(b) Calculate frequencies

(c) Determine which signal has higher frequency

Solution:

(a) Standard units:

$$T_A = 2.5 \times 10^{-3}\,s = 0.0025\,s$$
$$T_B = 400 \times 10^{-6}\,s = 0.0004\,s$$

(b) Frequencies:

$$f_A = \frac{1}{T_A} = \frac{1}{0.0025} = 400\,Hz$$
$$f_B = \frac{1}{T_B} = \frac{1}{0.0004} = 2500\,Hz = 2.5\,kHz$$

(c) Signal B has higher frequency ($2.5\,kHz > 400\,Hz$)

2.4 Exercises

Exercise 2.1

A heart monitor shows 72 beats per minute. Calculate:

(a) Frequency in Hz

(b) Period in seconds

Exercise 2.2

A signal has a period of $40\,\mu s$. Determine:

(a) Frequency in kHz

(b) Number of cycles in 1 ms

Exercise 2.3

Classify the following as analog or digital signals:

(a) Temperature variation over a day

(b) Binary data from a computer

(c) Sound from a microphone

(d) Digital clock display

(e) Voltage from a sensor

Exercise 2.4

The speed of an old modem is $56,000\,bps$ (bits per second). A character is coded using 8 bits (1 byte).

(a) How many characters are transferred per second?

(b) How many characters are transferred per minute?

(c) If a document contains 50,000 characters, how long will it take to transfer?

2.5 Solutions

Solution 2.1

(a) Convert beats per minute to Hz:

$$f = \frac{72\,\text{beats}}{60\,\text{seconds}} = 1.2\,Hz$$

(b) Period:

$$T = \frac{1}{f} = \frac{1}{1.2} = 0.833\,s$$

Solution 2.2

(a) Frequency:

$$f = \frac{1}{T} = \frac{1}{40 \times 10^{-6}} = 25,000\,Hz = 25\,kHz$$

(b) Number of cycles in 1 ms:

$$\text{Cycles} = f \times t = 25,000 \times 0.001 = 25\,\text{cycles}$$

Solution 2.3

(a) Temperature variation: Analog (continuous)

(b) Binary data: Digital (discrete)

(c) Sound from microphone: Analog (continuous)

(d) Digital clock display: Digital (discrete)

(e) Voltage from sensor: Analog (continuous)

Solution 2.4

(a) Characters per second:

$$\frac{56,000\,\text{bits/s}}{8\,\text{bits/character}} = 7,000\,\text{characters/s}$$

(b) Characters per minute:

$$7,000 \times 60 = 420,000\,\text{characters/minute}$$

(c) Transfer time for 50,000 characters:

$$t = \frac{50,000}{7,000} = 7.14\,\text{seconds}$$

2.6 Chapter Exam

Part 1: Theory (5 Points)

1. Define frequency and period, and state their mathematical relationship.
2. Explain the difference between analog and digital signals with examples.
3. What is modulation and why is it important in communications?

Part 2: Calculations (10 Points)

1. A signal generator produces 2,500 cycles in 0.5 seconds.
   (a) Calculate the frequency in kHz.
   (b) Determine the period in microseconds.
   (c) How many cycles occur in 10 ms?
2. A broadband modem can download a 1.5 GB file in 25 minutes.
   (a) Calculate the download speed in MB/s.
   (b) Convert this to bits per second (1 byte = 8 bits).
   (c) If a webpage is 2 MB, how long will it take to download?

Part 3: Signal Analysis (5 Points)

Two sound signals A and B are tested on a patient. Signal A has period $T_A = 2\,ms$ and is not heard. Signal B has frequency $f_B = 5\,kHz$ and is heard clearly.

1. Calculate f_A and T_B.
2. Does the patient have high-frequency or low-frequency hearing loss? Justify.
3. If human hearing range is 20 Hz to 20 kHz, are both signals within range?

2.7 Exam Solution

Part 1: Theory (5 Points)

1. **Frequency and Period:**
   - **Frequency (f):** Number of cycles or oscillations per second. Measured in Hertz (Hz).
   - **Period (T):** Time taken for one complete cycle or oscillation. Measured in seconds (s).
   - **Mathematical Relationship:**
   $$f = \frac{1}{T} \quad \text{or} \quad T = \frac{1}{f}$$
   Frequency and period are inversely proportional.
2. **Difference between Analog and Digital Signals:**
   - **Analog Signals:**
     - Continuous signals that can have infinite values within a range
     - Represent physical measurements (temperature, sound, light)
     - **Examples:** Voice on a telephone line, radio waves, analog thermometer reading
     - Susceptible to noise and distortion
   - **Digital Signals:**
     - Discrete signals that have only specific values (usually 0 and 1)
     - Represent information as binary data
     - **Examples:** Computer data, digital audio (MP3), digital TV signal
     - More resistant to noise, easier to store and process
3. **Modulation in Communications:**
   - **Definition:** Process of varying one or more properties of a carrier signal (amplitude, frequency, or phase) with a modulating signal (information signal)
   - **Importance:**
     (a) **Frequency Translation:** Allows transmission of low-frequency signals at higher frequencies suitable for transmission
     (b) **Multiplexing:** Enables multiple signals to share a single transmission channel
     (c) **Antenna Size Reduction:** Higher frequencies require smaller antennas
     (d) **Signal Quality:** Reduces interference and improves signal-to-noise ratio
     (e) **Bandwidth Efficiency:** Allows efficient use of available frequency spectrum
   - **Types:** AM (Amplitude Modulation), FM (Frequency Modulation), PM (Phase Modulation)

Part 2: Calculations (10 Points)

1. **Signal Generator Analysis:**
   (a) **Frequency in kHz:**
   $$f = \frac{\text{Number of cycles}}{\text{Time}} = \frac{2500}{0.5} = 5000\,\text{Hz}$$
   Convert to kHz:
   $$f = \frac{5000}{1000} = 5\,\text{kHz}$$
   (b) **Period in microseconds:**
   $$T = \frac{1}{f} = \frac{1}{5000} = 0.0002\,\text{s}$$
   Convert to microseconds:
   $$T = 0.0002 \times 1,000,000 = 200\,\mu\text{s}$$

(c) **Cycles in 10 ms:** Convert 10 ms to seconds:

$$10\,\text{ms} = 0.01\,\text{s}$$

Number of cycles:

$$\text{Cycles} = f \times \text{Time} = 5000 \times 0.01 = 50\,\text{cycles}$$

2. **Broadband Modem Analysis:**

(a) **Download speed in MB/s:** File size: 1.5 GB = 1500 MB Time: 25 minutes = 25 Œ 60 = 1500 seconds

$$\text{Speed} = \frac{\text{File size}}{\text{Time}} = \frac{1500\,\text{MB}}{1500\,\text{s}} = 1\,\text{MB/s}$$

(b) **Speed in bits per second:**

$$1\,\text{MB/s} = 1 \times 8 = 8\,\text{Mb/s} \quad \text{(Megabits per second)}$$

Convert to bits per second:

$$8\,\text{Mb/s} = 8 \times 1,000,000 = 8,000,000\,\text{bps}$$

(c) **Time to download 2 MB webpage:**

$$\text{Time} = \frac{\text{File size}}{\text{Speed}} = \frac{2\,\text{MB}}{1\,\text{MB/s}} = 2\,\text{seconds}$$

Part 3: Signal Analysis (5 Points)

1. **Calculate f_A and T_B:**

For Signal A:

$$T_A = 2\,\text{ms} = 0.002\,\text{s}$$

$$f_A = \frac{1}{T_A} = \frac{1}{0.002} = 500\,\text{Hz}$$

For Signal B:

$$f_B = 5\,\text{kHz} = 5000\,\text{Hz}$$

$$T_B = \frac{1}{f_B} = \frac{1}{5000} = 0.0002\,\text{s} = 0.2\,\text{ms}$$

2. **Determine type of hearing loss:**

Signal A: $f_A = 500\,\text{Hz}$ (low frequency) NOT heard

Signal B: $f_B = 5000\,\text{Hz}$ (high frequency) HEARD clearly

Diagnosis: The patient has **low-frequency hearing loss**.

Justification: The patient cannot hear the low-frequency signal (500 Hz) but can hear the high-frequency signal (5 kHz) clearly. This indicates reduced sensitivity to low-frequency sounds.

3. **Check if signals are within human hearing range:**

Human hearing range: 20 Hz to 20,000 Hz (20 kHz)

Signal A: $f_A = 500\,\text{Hz}$

$$20\,\text{Hz} \leq 500\,\text{Hz} \leq 20,000\,\text{Hz} \quad \text{YES, within range}$$

Signal B: $f_B = 5000\,\text{Hz} = 5\,\text{kHz}$

$$20\,\text{Hz} \leq 5000\,\text{Hz} \leq 20,000\,\text{Hz} \quad \text{YES, within range}$$

Conclusion: Both signals are within the normal human hearing range. Signal A (500 Hz) should be audible to a person with normal hearing, but this patient cannot hear it, confirming the low-frequency hearing loss diagnosis.

Chapter 3

Computer Architecture

3.1 Theoretical Foundation

Computer System Components

Von Neumann Architecture

The basic computer architecture consists of:

1. **CPU** (Central Processing Unit): Executes instructions
2. **Memory**: Stores programs and data
3. **I/O Devices**: Interface with external world
4. **Buses**: Communication pathways

Memory Hierarchy

Memory Characteristics

Memory Type	Speed	Size	Cost/bit
Registers	Fastest	Smallest	Highest
Cache (L1/L2)	Very Fast	Small	High
RAM	Fast	Medium	Medium
Hard Disk	Slow	Large	Low

Processor Components

CPU Functional Units

$$\text{CPU} = \text{Control Unit} + \text{ALU} + \text{Registers}$$

- **Control Unit**: Fetches, decodes, and executes instructions
- **ALU**: Performs arithmetic and logical operations
- **Registers**: Fast temporary storage (PC, IR, ACC, etc.)

3.2 Key Technical Insights

- Clock speed determines how many instructions per second a CPU can execute.

- Data bus width affects how much data can be transferred at once.
- Cache memory reduces the processor-memory speed gap.
- Parallel processing increases throughput but adds complexity.

3.3 Worked Examples

Example 1: Memory Capacity Conversion

Problem: Convert the following memory capacities:

(a) $13\,MB$ to bytes

(b) $2.3\,GB$ to MB

(c) $1,435\,TB$ to GB

Solution:

(a) $13\,MB = 13 \times 2^{20}\,bytes = 13 \times 1,048,576 = 13,631,488\,bytes$

(b) $2.3\,GB = 2.3 \times 2^{10}\,MB = 2.3 \times 1024 = 2355.2\,MB$

(c) $1,435\,TB = 1,435 \times 2^{10}\,GB = 1,435 \times 1024 = 1,469,440\,GB$

Example 2: Bus Performance Calculation

Problem: A PCI bus has 64-bit width and operates at 66 MHz. Calculate:

(a) Theoretical transfer rate in MB/s

Solution:

(a) Transfer rate calculation:

$$\text{Rate} = \frac{\text{Bus width} \times \text{Frequency}}{8\,\text{bits/byte}}$$

$$\text{Rate} = \frac{64\,\text{bits} \times 66 \times 10^6\,\text{Hz}}{8} = 528 \times 10^6\,\text{bytes/s} = 528\,MB/s$$

3.4 Exercises

Exercise 3.1

Define the following terms:

(a) Motherboard

(b) Chipset (Northbridge/Southbridge)

(c) BIOS

(d) Bus

Exercise 3.2

Complete the bus comparison table:

Bus Type	Width (bits)	Frequency (MHz)	Rate (MB/s)
ISA	16	8.33	?
AGP	32	66	?
PCI	64	33	?
PCI-X	64	266	?

Exercise 3.3

A processor has clock speed of 3.2 GHz and can execute 4 instructions per cycle (IPC).

(a) Calculate instructions per second (IPS)

(b) Express in MIPS (Millions of Instructions Per Second)

(c) If a program has 5×10^9 instructions, how long will it take to execute?

Exercise 3.4

Classify the following memories by speed (fastest to slowest) and size (smallest to largest): RAM, Registers, L2 Cache, Hard Disk, L1 Cache, CD-ROM

3.5 Solutions

Solution 3.1

(a) **Motherboard**: Main circuit board connecting all computer components

(b) **Chipset**: Set of chips that manage data flow between processor, memory, and peripherals

- Northbridge: High-speed connections (CPU, RAM, GPU)
- Southbridge: Lower-speed I/O (USB, SATA, audio)

(c) **BIOS**: Basic Input/Output System - firmware that initializes hardware during boot

(d) **Bus**: Communication system that transfers data between components

Solution 3.2

Transfer rate formula: Rate $= \frac{\text{Width} \times \text{Frequency}}{8}$

1. ISA: $\frac{16 \times 8.33}{8} = 16.66\,MB/s$
2. AGP: $\frac{32 \times 66}{8} = 264\,MB/s$
3. PCI: $\frac{64 \times 33}{8} = 264\,MB/s$
4. PCI-X: $\frac{64 \times 266}{8} = 2,128\,MB/s$

Completed table:

Bus Type	Width (bits)	Frequency (MHz)	Rate (MB/s)
ISA	16	8.33	16.66
AGP	32	66	264
PCI	64	33	264
PCI-X	64	266	2128

Solution 3.3

(a) Instructions per second:

$$\text{IPS} = \text{Clock speed} \times \text{IPC} = 3.2 \times 10^9 \times 4 = 12.8 \times 10^9 \text{ instructions/s}$$

(b) In MIPS:

$$12.8 \times 10^9 \text{ IPS} = 12,800 \text{ MIPS}$$

(c) Execution time:

$$t = \frac{\text{Instructions}}{\text{IPS}} = \frac{5 \times 10^9}{12.8 \times 10^9} = 0.3906 \text{ seconds}$$

Solution 3.4

- By speed (fastest to slowest): Registers > L1 Cache > L2 Cache > RAM > Hard Disk > CD-ROM
- By size (smallest to largest): Registers < L1 Cache < L2 Cache < RAM < CD-ROM < Hard Disk

3.6 Chapter Exam

Part 1: Theory (5 Points)

1. Explain the difference between RISC and CISC architectures.
2. Describe the memory hierarchy and why it exists.
3. What are the main components of a CPU and their functions?

Part 2: Calculations (10 Points)

1. Convert the following memory capacities:
   (a) $4.7\,GB$ to MB
   (b) $8\,TB$ to GB
   (c) $512\,MB$ to bytes
   (d) $16\,GB$ to KB
2. A processor has the following specifications:
   - Clock speed: 2.4 GHz
   - IPC: 3.5
   - Cache: L1 = 64 KB, L2 = 256 KB, L3 = 8 MB

   Calculate:
   (a) Instructions per second
   (b) Execution time for 10^{10} instructions

Part 3: Architecture Analysis (5 Points)

Compare two systems:

- System A: 3.0 GHz, 2 IPC, 4 GB RAM
- System B: 2.4 GHz, 3 IPC, 8 GB RAM

1. Which has higher IPS? Show calculations.
2. For memory-intensive applications, which might perform better and why?
3. What other factors might affect overall performance?

3.7 Exam Solution

Part 1: Theory (5 Points)

1. **RISC vs CISC Architectures:**
   - **RISC (Reduced Instruction Set Computer):**
     - Uses simple, fixed-length instructions
     - Smaller instruction set (typically 100-200 instructions)
     - Instructions execute in one clock cycle
     - Emphasizes pipelining for performance
     - Relies on compiler for optimization
     - **Examples:** ARM, MIPS, PowerPC, RISC-V
   - **CISC (Complex Instruction Set Computer):**
     - Uses complex, variable-length instructions
     - Larger instruction set (200+ instructions)
     - Instructions may take multiple clock cycles
     - Single instruction can perform complex operations
     - Hardware handles complexity
     - **Examples:** x86, Intel Pentium, AMD processors
2. **Memory Hierarchy and Its Purpose:**
   - **Memory Hierarchy (from fastest to slowest, smallest to largest):**
     (a) Registers (inside CPU)
     (b) Cache (L1, L2, L3)
     (c) Main Memory (RAM)
     (d) Secondary Storage (SSD/HDD)
     (e) Tertiary Storage (Tape, Optical)
   - **Why it exists:**
     (a) **Speed vs Cost Trade-off:** Faster memory is more expensive per byte
     (b) **Locality of Reference:**
       - Temporal Locality: Recently accessed data likely to be accessed again
       - Spatial Locality: Data near accessed data likely to be accessed soon
     (c) **Performance Optimization:** Keeps frequently used data in fast memory
     (d) **Cost Efficiency:** Balances performance with cost constraints
3. **Main CPU Components and Functions:**
   - **Control Unit (CU):**
     - Directs operation of the processor
     - Decodes instructions
     - Coordinates activities of other units
     - Manages data flow between components
   - **Arithmetic Logic Unit (ALU):**
     - Performs arithmetic operations (addition, subtraction, etc.)
     - Performs logical operations (AND, OR, NOT, etc.)
     - Performs bit-shifting operations
     - Contains flags for comparison results
   - **Registers:**
     - Small, fast storage locations inside CPU
     - Hold data being processed
     - Types: General purpose, special purpose (PC, SP, IR)

- **Cache Memory:**
  - Fast memory between CPU and RAM
  - Stores frequently used data/instructions
  - Levels: L1 (fastest), L2, L3 (largest)
- **Bus Interface Unit (BIU):**
  - Manages communication between CPU and other components
  - Handles data transfer on system bus

Part 2: Calculations (10 Points)

1. **Memory Capacity Conversions:**

   (a) $4.7\,GB$ to MB:
   $$4.7 \times 1024 = 4812.8\,MB$$

   (b) $8\,TB$ to GB:
   $$8 \times 1024 = 8192\,GB$$

   (c) $512\,MB$ to bytes:
   $$512 \times 1024 \times 1024 = 536,870,912\,bytes$$

   (d) $16\,GB$ to KB:
   $$16 \times 1024 \times 1024 = 16,777,216\,KB$$

2. **Processor Performance Calculations:**

   (a) **Instructions per second:**

   $$\begin{aligned}\text{Clock speed} &= 2.4\,GHz = 2.4 \times 10^9\,Hz\\ \text{IPC} &= 3.5\\ \text{IPS} &= \text{Clock speed} \times \text{IPC}\\ &= 2.4 \times 10^9 \times 3.5\\ &= 8.4 \times 10^9\,\text{instructions/second}\\ &= 8.4\,\text{billion IPS}\end{aligned}$$

   (b) **Execution time for 10^{10} instructions:**

   $$\begin{aligned}\text{Instructions} &= 10^{10} = 10,000,000,000\\ \text{Time} &= \frac{\text{Instructions}}{\text{IPS}}\\ &= \frac{10^{10}}{8.4 \times 10^9}\\ &= 1.1905\,\text{seconds}\end{aligned}$$

   Alternative calculation using CPI:

   $$\begin{aligned}\text{CPI} &= \frac{1}{\text{IPC}} = \frac{1}{3.5} = 0.2857\,\text{cycles/instruction}\\ \text{Total cycles} &= 10^{10} \times 0.2857 = 2.857 \times 10^9\,\text{cycles}\\ \text{Time} &= \frac{\text{Cycles}}{\text{Clock frequency}}\\ &= \frac{2.857 \times 10^9}{2.4 \times 10^9} = 1.1904\,\text{seconds}\end{aligned}$$

Part 3: Architecture Analysis (5 Points)

1. **IPS Comparison:**

   - **System A:** 3.0 GHz, IPC = 2

   $$IPS_A = 3.0 \times 10^9 \times 2 = 6.0 \times 10^9 \text{ IPS}$$

   - **System B:** 2.4 GHz, IPC = 3

   $$IPS_B = 2.4 \times 10^9 \times 3 = 7.2 \times 10^9 \text{ IPS}$$

   Conclusion: System B has higher IPS (7.2 billion vs 6.0 billion).

2. **Performance for Memory-Intensive Applications:**

   System B would likely perform better for memory-intensive applications because:

   (a) **More RAM:** 8 GB vs 4 GB allows more data to be kept in memory
   (b) **Reduced Disk Access:** Less need for virtual memory/page file usage
   (c) **Faster Processing:** Higher IPS (7.2 vs 6.0 billion) helps with memory operations
   (d) **Better Cache Utilization:** Although not specified, higher IPC often indicates better cache design

3. **Other Performance Factors:**

   - **Cache Size and Design:** Larger/faster cache reduces memory latency
   - **Memory Speed:** RAM frequency (MHz) and timings (CAS latency)
   - **Bus Speed:** Front-side bus, memory bus speeds
   - **Number of Cores:** Multi-core processing capability
   - **Pipeline Design:** Depth and efficiency of instruction pipeline
   - **Branch Prediction:** Accuracy of branch prediction algorithms
   - **Superscalar Architecture:** Ability to execute multiple instructions simultaneously
   - **Memory Type:** DDR3, DDR4, DDR5 differences
   - **Storage Speed:** SSD vs HDD performance
   - **Operating System:** Efficiency of memory management and scheduling
   - **Application Optimization:** How well software utilizes hardware features

Summary: While System B has higher theoretical IPS and more RAM, real-world performance depends on the specific application, how well it's optimized, and the overall system configuration including cache, memory speed, and other architectural features.

Chapter 4

Operating Systems and Networks

4.1 Theoretical Foundation

Operating System Functions

OS Core Functions

1. **Process Management**: Creation, scheduling, termination
2. **Memory Management**: Allocation, protection, virtual memory
3. **File System Management**: Organization, access control
4. **Device Management**: Driver interface, I/O scheduling
5. **Security and Protection**: User authentication, access control

Process States

Process State Transitions

State	Description
New	Process being created
Ready	Waiting for CPU allocation
Running	Executing on CPU
Waiting	Waiting for I/O or event
Terminated	Finished execution

Network Classification

Network Types by Coverage

- **PAN**: Personal Area Network (10 m)
- **LAN**: Local Area Network (1 km)
- **MAN**: Metropolitan Area Network (10 km)
- **WAN**: Wide Area Network (100+ km)

4.2 Key Technical Insights

- Time-sharing systems allow multiple users to share computer resources.

- Virtual memory extends physical memory using disk storage.
- Network protocols ensure reliable data transmission.
- Routing tables determine optimal paths for data packets.

4.3 Worked Examples

Example 1: Process Scheduling

Problem: A system uses Round Robin scheduling with time quantum = 20 ms. Three processes have burst times:

- P1: 50 ms
- P2: 30 ms
- P3: 20 ms

Calculate completion times assuming all arrive at time 0.

Solution:

1. Time 0-20: P1 runs (remaining: 30 ms)
2. Time 20-40: P2 runs (remaining: 10 ms)
3. Time 40-60: P3 runs (completes at 60 ms)
4. Time 60-80: P1 runs (remaining: 10 ms)
5. Time 80-90: P2 runs (completes at 90 ms)
6. Time 90-100: P1 runs (completes at 100 ms)

Completion times: P1=100 ms, P2=90 ms, P3=60 ms

Example 2: Network Classification

Problem: Classify each scenario:

(a) Computers in a university campus

(b) Connecting smartphones via Bluetooth

(c) Bank branches across a country

(d) Computers in different cities of a province

Solution:

(a) University campus: LAN

(b) Smartphones via Bluetooth: PAN

(c) Bank branches nationwide: WAN

(d) Cities in a province: MAN

4.4 Exercises

Exercise 4.1

Define the following OS concepts:

(a) Multi-programming

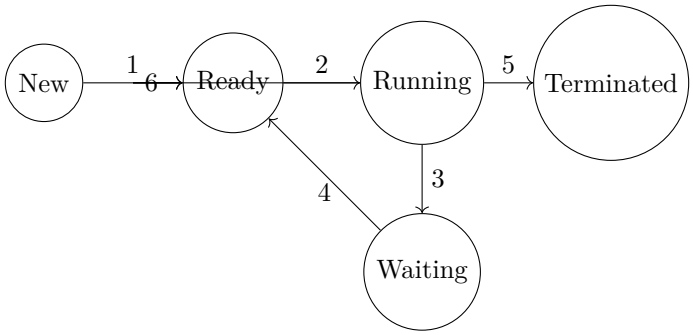
(b) Time-sharing

(c) Batch processing

(d) Real-time system

Exercise 4.2

For the process state diagram below, identify what each transition represents:



Exercise 4.3

Identify the network device based on description:

(a) Forwards packets between networks using routing tables

(b) Connects devices in a LAN, filters and forwards frames

(c) Simple device that repeats signals to all ports

(d) Connects different network types (e.g., Ethernet to Wi-Fi)

Exercise 4.4

A company needs to network its offices:

- Main office: 50 computers in one building
- Branch office: 20 computers in another city
- Field employees: Laptops and smartphones

Recommend network types for each and justify.

4.5 Solutions

Solution 4.1

(a) **Multi-programming**: Multiple programs in memory simultaneously, CPU switches between them

(b) **Time-sharing**: Multiple users share system resources with time slices

(c) **Batch processing**: Jobs collected and processed in batches without user interaction

(d) **Real-time system**: Guaranteed response within strict time constraints

Solution 4.2

1. Transition 1: Process admitted to ready queue
2. Transition 2: Scheduler dispatches process to CPU
3. Transition 3: Process requests I/O or waits for event
4. Transition 4: I/O completion or event occurs
5. Transition 5: Process completes execution
6. Transition 6: Time slice expires or higher priority process arrives

Solution 4.3

(a) Router

(b) Switch

(c) Hub

(d) Gateway or Bridge

Solution 4.4

1. Main office (50 computers in one building): LAN (Ethernet)
2. Branch office in another city: WAN (using leased lines or VPN over Internet)
3. Field employees: PAN for personal devices, mobile networks for connectivity

4.6 Chapter Exam

Part 1: Theory (5 Points)

1. What are the main functions of an operating system?
2. Explain process scheduling algorithms (FCFS and RR).
3. Differentiate between LAN, MAN, and WAN.

Part 2: Analysis (10 Points)

1. Three processes arrive at times and have burst times:

Process	Arrival Time	Burst Time
P1	0	8 ms
P2	1	4 ms
P3	2	9 ms

   Calculate for FCFS scheduling:

   (a) Completion times
   (b) Turnaround times
   (c) Waiting times
   (d) Average waiting time

2. A network connects:

   - Computers in a 5-story building
   - Smartphones of employees
   - Remote office 500 km away
   - City-wide surveillance cameras

   Identify network type for each.

Part 3: Design Problem (5 Points)

Design a network for a university with:

- Main campus: 10 buildings, 1000 computers
- Branch campus: 50 km away, 200 computers
- Student dormitories: Wireless access needed

Specify:

1. Network types for different areas
2. Required networking devices
3. Security considerations

4.7 Exam Solution

Part 1: Theory (5 Points)

1. **Main Functions of an Operating System:**
   - **Process Management:**
     - Process creation, scheduling, and termination
     - Inter-process communication
     - Process synchronization
     - Deadlock handling
   - **Memory Management:**
     - Allocation and deallocation of memory
     - Virtual memory management
     - Memory protection
     - Paging and segmentation
   - **File System Management:**
     - File creation, deletion, and organization
     - Directory management
     - File access control
     - Disk space management
   - **Device Management:**
     - Device drivers
     - I/O operations management
     - Device allocation and deallocation
     - Buffering and caching
   - **Security and Protection:**
     - User authentication and authorization
     - Access control lists
     - Protection against malware
     - Data encryption
   - **User Interface:**
     - Command-line interface (CLI)
     - Graphical user interface (GUI)
     - Application programming interface (API)
2. **Process Scheduling Algorithms:**
   - **FCFS (First-Come, First-Served):**
     - Processes are executed in order of arrival
     - Non-preemptive algorithm
     - Simple to implement but can cause convoy effect
     - May lead to poor average waiting time
     - Example: If processes arrive P1, P2, P3, they execute in that order
   - **RR (Round Robin):**
     - Each process gets a fixed time quantum (time slice)
     - Preemptive algorithm
     - Each process gets CPU time, then moves to back of queue
     - Fair to all processes
     - Good for time-sharing systems
     - Example: Time quantum = 4ms, processes share CPU in circular fashion

3. **LAN, MAN, and WAN Differences:**

LAN (Local Area Network)	**MAN (Metropolitan Area Network)**	**WAN (Wide Area Network)**
Small geographical area (Home, office, building)	City-wide coverage (Multiple buildings/campuses)	Large geographical area (Countries, continents)
High speed (1 Gbps to 10 Gbps)	Medium speed (100 Mbps to 1 Gbps)	Lower speed (1 Mbps to 100 Mbps)
Low latency	Medium latency	High latency
Low cost	Medium cost	High cost
Ethernet, Wi-Fi	Microwave, fiber optics	Fiber optics, satellite
Owned by single organization	Owned by organization or ISP	Multiple organizations, ISPs
Examples: Office network, home network	**Examples:** City-wide CCTV, university campus	**Examples:** Internet, bank networks

Part 2: Analysis (10 Points)

1. **FCFS Scheduling Analysis:**

Process	**Arrival Time**	**Burst Time**	**Completion Time**	**Turnaround Time**	**Waiting Time**
P1	0	8	8	8	0
P2	1	4	12	11	7
P3	2	9	21	19	10

(a) **Completion Times:**

P1: Starts at 0, completes at $0 + 8 = 8$ ms
P2: Starts at 8, completes at $8 + 4 = 12$ ms
P3: Starts at 12, completes at $12 + 9 = 21$ ms

(b) **Turnaround Times:**

P1: $8 - 0 = 8$ ms
P2: $12 - 1 = 11$ ms
P3: $21 - 2 = 19$ ms

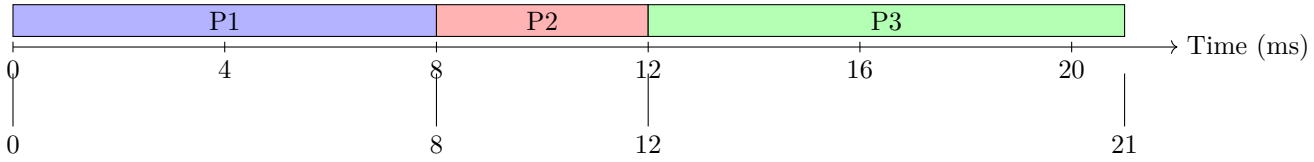
(c) **Waiting Times:**

P1: 0 ms (starts immediately)
P2: $8 - 1 = 7$ ms
P3: $12 - 2 = 10$ ms

(d) **Average Waiting Time:**

$$\text{Average} = \frac{0 + 7 + 10}{3} = \frac{17}{3} = 5.67 \text{ ms}$$

Gantt Chart:



2. **Network Type Identification:**

(a) **Computers in a 5-story building:**

- **Type:** LAN (Local Area Network)
- **Reason:** Limited geographical area within one building
- **Technology:** Typically Ethernet or Wi-Fi

(b) **Smartphones of employees:**

- **Type:** PAN (Personal Area Network) or WLAN (Wireless LAN)
- **Reason:** Personal devices within short range
- **Technology:** Bluetooth (PAN) or Wi-Fi (WLAN)

(c) **Remote office 500 km away:**

- **Type:** WAN (Wide Area Network)
- **Reason:** Large geographical distance between locations
- **Technology:** VPN over internet, leased lines

(d) **City-wide surveillance cameras:**

- **Type:** MAN (Metropolitan Area Network)
- **Reason:** Covers an entire city or metropolitan area
- **Technology:** Fiber optic cables, microwave links

Part 3: Design Problem (5 Points)

University Network Design:

1. **Network Types for Different Areas:**
   - **Main Campus (10 buildings, 1000 computers):**
     - **Type:** Campus Area Network (CAN) - multiple interconnected LANs
     - **Infrastructure:** Wired Ethernet (Cat 6/6A) for fixed workstations
     - **Backbone:** Fiber optic connections between buildings
   - **Individual Buildings:**
     - **Type:** LAN (Local Area Network)
     - **Structure:** Hierarchical with access, distribution, and core layers
   - **Student Dormitories:**
     - **Type:** WLAN (Wireless Local Area Network)
     - **Technology:** Wi-Fi 6/6E (802.11ax) for high-density coverage
     - **Coverage:** Multiple access points per floor
   - **Branch Campus (50 km away):**
     - **Type:** WAN (Wide Area Network) connection
     - **Technology:** Leased line (E1/T1), MPLS, or VPN over internet
2. **Required Networking Devices:**
   - **Core Layer:**
     - Core switches (Layer 3) for high-speed routing
     - Firewall for network security
     - Routers for WAN connectivity
   - **Distribution Layer:**
     - Distribution switches in each building
     - Network controllers for wireless access points
   - **Access Layer:**
     - Access switches for wired connections
     - Wireless access points (APs) for Wi-Fi coverage
     - Network Interface Cards (NICs) in computers
   - **Specialized Devices:**

  - Load balancers for web servers
  - VPN concentrators for remote access
  - Intrusion Prevention Systems (IPS)
  - Network monitoring servers

3. **Security Considerations:**

   - **Network Segmentation:**
     - Separate VLANs for different user groups (students, faculty, admin)
     - Isolate critical servers (finance, HR) in secure VLANs
     - Guest network for visitors
   - **Access Control:**
     - 802.1X authentication for network access
     - Role-based access control (RBAC)
     - MAC address filtering for sensitive areas
   - **Data Protection:**
     - Encryption for wireless networks (WPA3)
     - VPN for remote access to internal resources
     - SSL/TLS for web applications
   - **Monitoring and Defense:**
     - Intrusion Detection/Prevention Systems (IDS/IPS)
     - Security Information and Event Management (SIEM)
     - Regular security audits and vulnerability scans
     - DDoS protection
   - **Physical Security:**
     - Secure server rooms with access control
     - Camera surveillance for network equipment areas
     - UPS for power backup
   - **Policies and Compliance:**
     - Acceptable Use Policy (AUP) for all users
     - Regular security awareness training
     - Compliance with data protection regulations

Chapter 5

Electronic Components

5.1 Theoretical Foundation

Component Classification

Active vs Passive Components

- **Active**: Require external power, can amplify signals
  - Transistors, Diodes, ICs, Vacuum tubes
- **Passive**: Do not require external power, cannot amplify
  - Resistors, Capacitors, Inductors, Transformers

Diode Characteristics

Diode Equation

The Shockley diode equation describes current-voltage relationship:

$$I = I_S \left(e^{\frac{V}{nV_T}} - 1 \right)$$

where:

- I_S = Reverse saturation current
- $V_T = \frac{kT}{q} \approx 26\,mV$ at room temperature
- n = Ideality factor (1-2)

Transistor Operation

BJT Operating Regions

1. **Cutoff**: $I_B = 0$, $I_C = 0$ (OFF state)
2. **Active**: $I_C = \beta I_B$, used for amplification
3. **Saturation**: $V_{CE} \approx 0.2V$, used for switching (ON state)

5.2 Key Technical Insights

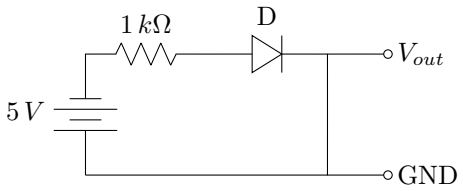
- Diodes conduct current only in one direction (forward bias).

- Transistors can amplify signals or act as switches.
- Capacitors store energy in electric fields.
- Inductors store energy in magnetic fields.
- Transformers transfer energy through electromagnetic induction.

5.3 Worked Examples

Example 1: Diode Circuit Analysis

Problem: For the circuit below with silicon diode ($V_D = 0.7V$), find V_{out}.



Solution: Assuming diode is forward biased:

$$V_{out} = 5V - V_D = 5 - 0.7 = 4.3V$$

Check: Diode is forward biased since anode is at higher potential than cathode.

Example 2: Transistor Biasing

Problem: For a BJT with $\beta = 100$, $V_{CC} = 12V$, $R_C = 1k\Omega$, $R_B = 100k\Omega$, find I_C and V_{CE}.
Solution:

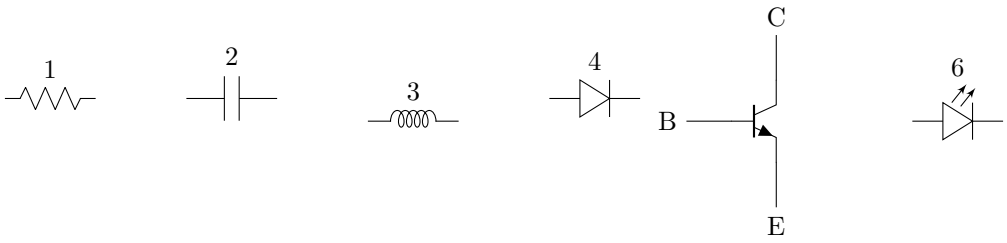
1. Base current:
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{100 \times 10^3} = 113\,\mu A$$
2. Collector current:
$$I_C = \beta I_B = 100 \times 113 \times 10^{-6} = 11.3\,mA$$
3. Collector-emitter voltage:
$$V_{CE} = V_{CC} - I_C R_C = 12 - (11.3 \times 10^{-3} \times 1000) = 0.7\,V$$

Since $V_{CE} \approx 0.7V$, transistor is in saturation region.

5.4 Exercises

Exercise 5.1

Identify these components from symbols:



Exercise 5.2

Classify as active or passive:

(a) Resistor

(b) Transistor

(c) Capacitor

(d) Diode

(e) Transformer

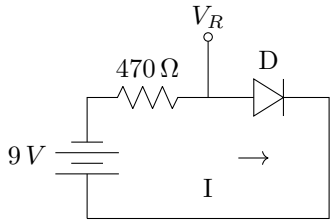
(f) Integrated Circuit

(g) LED

(h) Inductor

Exercise 5.3

For the diode circuit, calculate I and V_R. Assume silicon diode ($V_D = 0.7V$).



Exercise 5.4

A transistor amplifier has $V_{CC} = 15V$, $R_C = 2.2k\Omega$, $\beta = 120$. If $I_B = 50\mu A$, calculate:

(a) I_C

(b) V_{CE}

(c) Operating region

5.5 Solutions

Solution 5.1

1. Resistor
2. Capacitor
3. Inductor
4. Diode
5. Bipolar Junction Transistor (BJT)
6. Light Emitting Diode (LED)

Solution 5.2

(a) Resistor: Passive

(b) Transistor: Active

(c) Capacitor: Passive

(d) Diode: Active

(e) Transformer: Passive

(f) Integrated Circuit: Active

(g) LED: Active

(h) Inductor: Passive

Solution 5.3

1. Assuming forward bias, voltage across resistor:

$$V_R = 9V - 0.7V = 8.3V$$

2. Current through circuit:

$$I = \frac{V_R}{R} = \frac{8.3}{470} = 0.01766\,A = 17.66\,mA$$

3. Verification: Diode is forward biased since $9V > 0.7V$.

Solution 5.4

(a) Collector current:

$$I_C = \beta I_B = 120 \times 50 \times 10^{-6} = 6\,mA$$

(b) Collector-emitter voltage:

$$V_{CE} = V_{CC} - I_C R_C = 15 - (6 \times 10^{-3} \times 2200) = 15 - 13.2 = 1.8\,V$$

(c) Since $V_{CE} > 0.2V$ and $I_C = \beta I_B$, transistor is in active region.

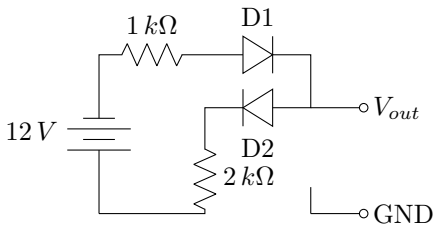
5.6 Chapter Exam

Part 1: Theory (5 Points)

1. Differentiate between active and passive components with examples.
2. Explain diode operation in forward and reverse bias.
3. Describe the three operating regions of a BJT.

Part 2: Circuit Analysis (10 Points)

1. For the circuit below, calculate V_{out} (Assume silicon diodes, $V_D = 0.7V$).



2. A transistor circuit has:
   - $V_{CC} = 10V$, $R_C = 1k\Omega$, $R_B = 220k\Omega$, $\beta = 150$

   Calculate:

   (a) I_B, I_C, V_{CE}
   (b) Operating region
   (c) Power dissipated in transistor

Part 3: Design Problem (5 Points)

Design a simple LED circuit with:

- Power supply: $9V$ battery
- LED: Forward voltage $2V$, maximum current $20mA$
- Include current-limiting resistor

1. Calculate required resistor value
2. Draw complete circuit diagram
3. Calculate power dissipated in resistor

5.7 Exam Solution

Part 1: Theory (5 Points)

1. **Active vs Passive Components:**

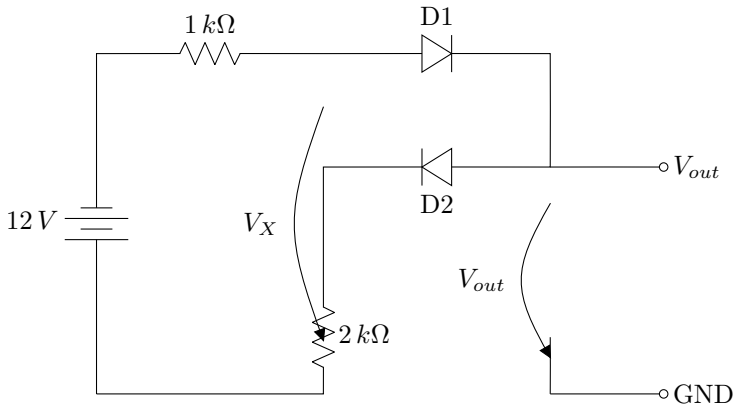
Active Components	Passive Components
• Can amplify signals • Can control current flow • Require external power source • Can provide power gain • Non-linear behavior	• Cannot amplify signals • Cannot control current flow • Do not require external power • Cannot provide power gain • Linear behavior (mostly)
Examples: • Transistors (BJT, MOSFET) • Diodes • Integrated Circuits (ICs) • Operational Amplifiers • Thyristors, TRIACs	**Examples:** • Resistors • Capacitors • Inductors • Transformers • Crystals, fuses

2. **Diode Operation:**
   - **Forward Bias:**
     - Positive terminal of battery connected to anode (P-type)
     - Negative terminal connected to cathode (N-type)
     - Depletion region narrows
     - Current flows when $V_{applied} > V_{threshold}$ (0.3V for Ge, 0.7V for Si)
     - Low resistance path for current
   - **Reverse Bias:**
     - Positive terminal of battery connected to cathode (N-type)
     - Negative terminal connected to anode (P-type)
     - Depletion region widens
     - Very small leakage current (μA range)
     - High resistance path (virtually open circuit)
     - Breakdown occurs at reverse breakdown voltage
   - **I-V Characteristic:**
     - Non-linear relationship
     - Forward current: $I = I_S(e^{V_D/V_T} - 1)$
     - Reverse saturation current I_S is very small
3. **BJT Operating Regions:**
   - **Active Region:**
     - Base-emitter junction: Forward biased
     - Base-collector junction: Reverse biased
     - Transistor acts as amplifier
     - $I_C = \beta I_B$
     - Used for linear amplification circuits
   - **Saturation Region:**
     - Base-emitter junction: Forward biased
     - Base-collector junction: Forward biased

  - Transistor acts as closed switch
  - $V_{CE} \approx 0.2V$ (saturation voltage)
  - I_C determined by external circuit, not by I_B
  - Used for switching applications (ON state)
- **Cut-off Region:**
  - Base-emitter junction: Reverse biased
  - Base-collector junction: Reverse biased
  - Transistor acts as open switch
  - $I_B \approx 0$, $I_C \approx 0$
  - Very small leakage currents
  - Used for switching applications (OFF state)
- **Reverse Active Region:**
  - Base-emitter junction: Reverse biased
  - Base-collector junction: Forward biased
  - Not commonly used (poor performance)

Part 2: Circuit Analysis (10 Points)

1. **Diode Circuit Analysis:**



Analysis:

(1) **Assume D1 is ON and D2 is OFF:**
- If D2 is OFF, no current through $2k\Omega$ resistor
- $V_X = 12V - V_{D1} = 12 - 0.7 = 11.3V$
- For D2 to be OFF: $V_{out} > V_X$
- But V_{out} is floating? Actually connected to GND through output terminal
- This assumption seems incorrect

(2) **Better approach: Analyze diode states**

Step 1: Consider D1
- Anode of D1 connected to V_X through $1k\Omega$
- Cathode connected to V_{out}
- For D1 to conduct: $V_X - V_{out} > 0.7V$

Step 2: Consider D2
- Anode of D2 connected to V_{out}
- Cathode connected to ground through $2k\Omega$
- For D2 to conduct: $V_{out} > 0.7V$

Step 3: Likely scenario: D1 OFF, D2 ON

- If D2 is ON: $V_{out} = 0.7V$
- Then voltage at D1 cathode $= 0.7V$
- For D1 to be OFF: $V_X < 0.7V + 0.7V = 1.4V$
- Let's check: Current through $2k\Omega = \frac{0.7V}{2k\Omega} = 0.35mA$
- This current comes from ground through D2
- No current through D1, so $V_X = 12V$ (through $1k\Omega$ with no current)
- But $V_X = 12V > 1.4V$, so D1 should be ON!
- Contradiction

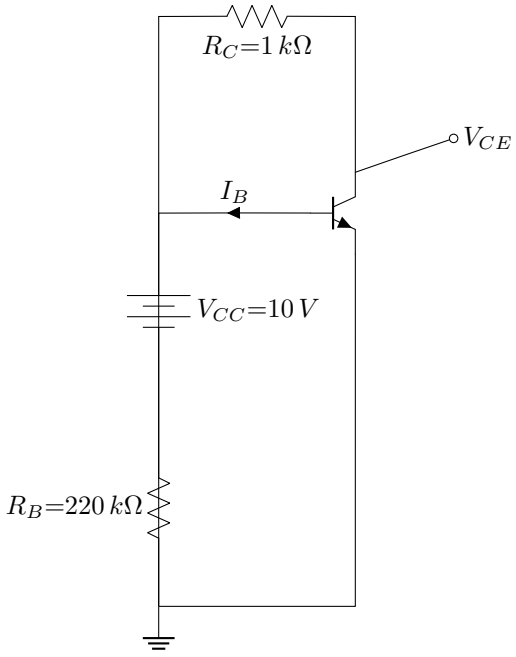
Step 4: Alternative: Both D1 and D2 ON

- If both diodes ON:
- $V_{out} = 0.7V$ (from D2)
- $V_X = V_{out} + 0.7V = 0.7 + 0.7 = 1.4V$ (from D1)
- Current through $1k\Omega$: $I_{R1} = \frac{12-1.4}{1k} = \frac{10.6}{1000} = 10.6mA$
- Current through $2k\Omega$: $I_{R2} = \frac{0.7}{2k} = 0.35mA$
- Current through D2: $I_{D2} = I_{R2} = 0.35mA$
- Current through D1: $I_{D1} = I_{R1} - I_{D2} = 10.6 - 0.35 = 10.25mA$
- Both diodes have forward current > 0, so assumption valid

Final Answer:

$$\boxed{V_{out} = 0.7V}$$

2. **Transistor Circuit Analysis:**



(a) **Calculate I_B, I_C, V_{CE}:**
Assume Active Region:

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B} \\ &= \frac{10 - 0.7}{220 \times 10^3} \\ &= \frac{9.3}{220,000} \\ &= 4.227 \times 10^{-5}\, A \\ &= 42.27\, \mu A \end{aligned}$$

$$\begin{aligned} I_C &= \beta \times I_B \\ &= 150 \times 42.27 \times 10^{-6} \\ &= 0.00634\,A \\ &= 6.34\,mA \end{aligned}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C \times R_C \\ &= 10 - (6.34 \times 10^{-3} \times 1000) \\ &= 10 - 6.34 \\ &= 3.66\,V \end{aligned}$$

(b) **Operating Region:**
Check saturation condition:

$$V_{CE(sat)} \approx 0.2V \quad \text{(typical for silicon)}$$

Our calculated $V_{CE} = 3.66V > 0.2V$, so:
Transistor is in ACTIVE REGION
Also check:

- $V_{BE} = 0.7V > 0$ (Forward biased ✓)
- $V_{CE} = 3.66V > V_{BE}$ (Reverse biased collector ✓)
- $I_C = \beta I_B$ relationship holds ✓

(c) **Power dissipated in transistor:**
Total power dissipation:

$$\begin{aligned} P_{total} &= V_{CE} \times I_C + V_{BE} \times I_B \\ &\approx V_{CE} \times I_C \quad \text{(since } V_{BE} \times I_B \text{ is small)} \end{aligned}$$

$$\begin{aligned} P_{total} &= 3.66 \times 6.34 \times 10^{-3} \\ &= 0.0232\,W \\ &= 23.2\,mW \end{aligned}$$

Collector power dissipation:

$$\begin{aligned} P_C &= V_{CE} \times I_C \\ &= 3.66 \times 6.34 \times 10^{-3} \\ &= 23.2\,mW \end{aligned}$$

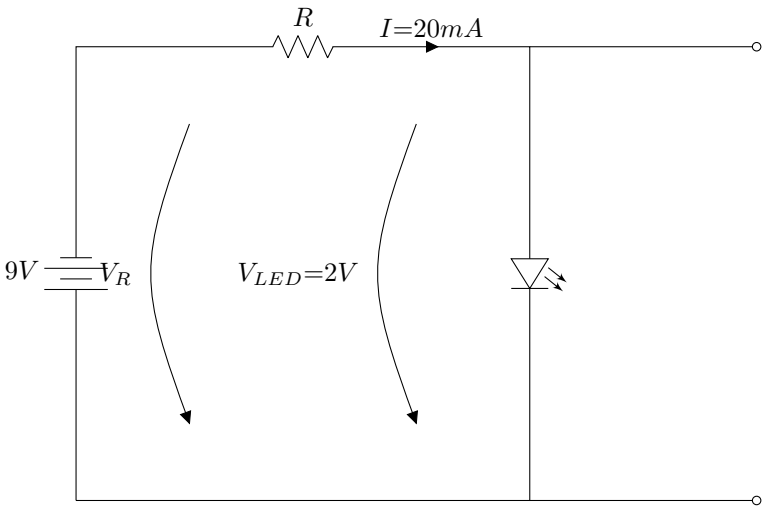
Base power dissipation:

$$\begin{aligned} P_B &= V_{BE} \times I_B \\ &= 0.7 \times 42.27 \times 10^{-6} \\ &= 29.6\,\mu W \end{aligned}$$

Part 3: Design Problem (5 Points)

LED Circuit Design:

1. **Required Resistor Value:**



Using Ohm's Law:

$$V_{supply} = V_R + V_{LED}$$
$$9 = V_R + 2 \Rightarrow V_R = 7V$$

Required resistance:

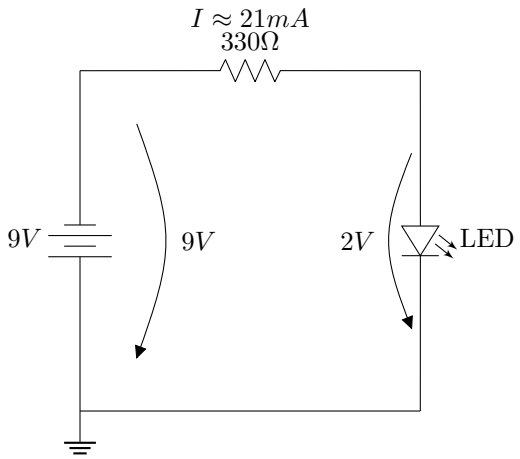
$$R = \frac{V_R}{I} = \frac{7}{0.020} = 350\,\Omega$$

Using standard resistor values:

- Calculated: 350Ω
- Nearest standard values: 330Ω or 390Ω
- Choose 330Ω for brighter LED (higher current)
- Check current with 330Ω: $I = \frac{7}{330} = 21.2mA$ (slightly above, but safe for most LEDs)
- Or choose 390Ω for more conservative design: $I = \frac{7}{390} = 17.9mA$

Final choice: $R = 330\Omega$ (standard value)

2. **Complete Circuit Diagram:**



3. **Power Dissipated in Resistor:**

   With $R = 330\Omega$:

$$I = \frac{9-2}{330} = \frac{7}{330} = 0.0212\,A = 21.2\,mA$$

   Power in resistor:

$$\begin{aligned} P_R &= I^2 \times R \\ &= (0.0212)^2 \times 330 \\ &= 0.000449 \times 330 \\ &= 0.148\,W \end{aligned}$$

   Or using voltage:

$$\begin{aligned} P_R &= \frac{V_R^2}{R} \\ &= \frac{7^2}{330} \\ &= \frac{49}{330} \\ &= 0.148\,W \end{aligned}$$

   Resistor specification:

   - Resistance: 330Ω
   - Power rating: At least 0.25W (use 0.5W for safety margin)
   - Tolerance: 5% (standard) or 1% for better precision

   LED power dissipation:

$$\begin{aligned} P_{LED} &= V_{LED} \times I \\ &= 2 \times 0.0212 \\ &= 0.0424\,W = 42.4\,mW \end{aligned}$$

   Total power from battery:

$$\begin{aligned} P_{total} &= V_{supply} \times I \\ &= 9 \times 0.0212 \\ &= 0.191\,W \end{aligned}$$

   Check: $P_R + P_{LED} = 0.148 + 0.0424 = 0.1904\,W \approx 0.191\,W$ ✓

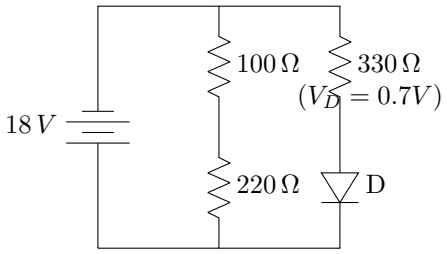
Chapter 6

Chapter Exam

6.1 Exam 1

Problem 1: Circuit Analysis (8 Points)

For the circuit shown:



Calculate:

(a) Total resistance

(b) Current through the 100 Ω resistor

(c) Voltage across the diode

(d) Power supplied by the battery

Problem 2: Signal Analysis (6 Points)

A signal has the equation: $v(t) = 5\sin(2\pi \times 1000t + \pi/4)$

(a) Determine amplitude, frequency, and phase

(b) Calculate period in milliseconds

(c) Find instantaneous voltage at $t = 0.25\,ms$

Problem 3: Computer Architecture (6 Points)

A computer system has:

- CPU: 3.6 GHz, 64-bit data bus
- Memory: 8 GB DDR4, 3200 MHz
- Cache: L1=64 KB, L2=256 KB, L3=8 MB

Calculate:

(a) Maximum theoretical memory bandwidth in GB/s

(b) Time to transfer 1 MB of data at maximum bandwidth

(c) Cache to main memory size ratio

6.2 Exam 2

Problem 1: Operating Systems (7 Points)

Three processes have the following characteristics:

Process	Arrival	Burst	Priority
P1	0	10	3
P2	1	4	1
P3	2	8	2

(Lower priority number = higher priority)

(a) Draw Gantt chart for Priority scheduling

(b) Calculate turnaround times

(c) Calculate waiting times

(d) Average waiting time

Problem 2: Network Design (7 Points)

Design a network for a small business with:

- Main office: 30 computers, 5 printers
- Branch office: 10 computers, 2 printers (50 km away)
- Mobile workers: 15 smartphones/tablets

Specify:

(a) Network types for each connection

(b) Required networking devices

(c) Addressing scheme considerations

Problem 3: Component Selection (6 Points)

Select appropriate components for:

(a) Voltage regulation from 12V to 5V

(b) Signal amplification with gain of 100

(c) Storing energy for backup power

(d) Converting AC to DC

(e) Protecting circuit from overvoltage

(f) Wireless communication between devices

6.3 Exam 3

Problem 1: Transistor Amplifier (8 Points)

Design a common-emitter amplifier with:

- $V_{CC} = 12V$
- Voltage gain $A_v \geq 50$
- Input impedance $Z_{in} \geq 1k\Omega$
- $\beta = 200$, $V_{BE} = 0.7V$

Calculate:

(a) Required R_C and R_E values

(b) Biasing resistors R_1 and R_2

(c) Input and output coupling capacitors for $f_{low} = 100Hz$

Problem 2: Digital System (6 Points)

A digital system processes 8-bit data with clock frequency 50 MHz.

(a) Calculate maximum data transfer rate

(b) If each instruction takes 4 clock cycles, calculate MIPS rating

(c) Design address decoding for 64 KB memory using 16-bit address bus

Problem 3: Integrated Design (6 Points)

Design a temperature monitoring system with:

- Sensor output: 0-5V for 0-100řC
- Microcontroller: 10-bit ADC, 3.3V reference
- Display: 16x2 LCD
- Alarm: Buzzer for temperatures >80řC

Specify:

(a) Required signal conditioning

(b) Resolution of temperature measurement

(c) Flowchart of control algorithm

Chapter 7

Exam Solutions

7.1 Exam 1 Solutions

Problem 1: Circuit Analysis

(a) Simplify the circuit:

- 220Ω and diode are in series: $R_{series} = 220 + 0.7/I$ (but diode voltage is fixed)
- Actually, diode has constant 0.7V drop when forward biased
- Check if diode is forward biased: Assume it is, then voltage at anode > cathode

Better approach: Use Thévenin equivalent or node analysis. Let V_A = voltage at diode anode.

From left branch: $I_1 = (18 - V_A)/100$ From right branch: $V_A = 0.7 + I_2 \times 220$ (diode drop + resistor) Also, $I_1 = I_2$ (series)

Solve: $(18 - V_A)/100 = (V_A - 0.7)/220$ $220(18 - V_A) = 100(V_A - 0.7)$ $3960 - 220V_A = 100V_A - 70$ $4030 = 320V_A$ $V_A = 12.59375V$

$I_1 = (18 - 12.59375)/100 = 0.0540625A = 54.06mA$

Total current from battery $= I_1 + I_3$ where $I_3 = V_A/330 = 12.59375/330 = 0.03816A$ Total current $= 54.06 + 38.16 = 92.22mA$

Total resistance seen by battery $= 18/0.09222 = 195.2\Omega$

(b) Current through $100\Omega = 54.06mA$

(c) Voltage across diode $= 0.7V$ (given)

(d) Power from battery $= 18 \times 0.09222 = 1.66W$

Problem 2: Signal Analysis

(a) From $v(t) = 5\sin(2\pi \times 1000t + \pi/4)$:

- Amplitude $= 5V$
- Frequency $= 1000Hz = 1kHz$
- Phase $= \pi/4$ radians $= 45°$

(b) Period $T = 1/f = 1/1000 = 0.001s = 1ms$

(c) At $t = 0.25ms = 0.00025s$: $v(0.00025) = 5\sin(2\pi \times 1000 \times 0.00025 + \pi/4) = 5\sin(2\pi \times 0.25 + \pi/4)$ $= 5\sin(\pi/2 + \pi/4) = 5\sin(3\pi/4) = 5 \times \sqrt{2}/2 = 3.5355V$

Problem 3: Computer Architecture

(a) Memory bandwidth: DDR4 3200 MHz transfers data on both clock edges (double data rate) Effective rate = $3200 \times 2 = 6400$ MT/s (Mega Transfers per second) 64-bit bus = 8 bytes Bandwidth = $6400 \times 8 = 51200$ MB/s = 51.2 GB/s

(b) Time for 1 MB transfer: $t = \text{size/bandwidth} = 1\,MB/51200\,MB/s = 1.95 \times 10^{-5} s = 19.5 \mu s$

(c) Cache ratio: Total cache = L1 + L2 + L3 = $64 + 256 + 8192 = 8512\,KB = 8.3125\,MB$ Main memory = $8\,GB = 8192\,MB$ Ratio = $8.3125/8192 \approx 0.001015 = 0.1015\%$

7.2 Exam 2 Solutions

Problem 1: Operating Systems

Priority scheduling (lower number = higher priority):

1. Time 0: P1 arrives (priority 3) - starts
2. Time 1: P2 arrives (priority 1) - preempts P1
3. Time 1-5: P2 runs (completes at time 5)
4. Time 5: P3 has priority 2 vs P1 priority 3, so P3 runs
5. Time 5-13: P3 runs (completes at time 13)
6. Time 13-23: P1 runs (completes at time 23)

Gantt chart: P1(0-1), P2(1-5), P3(5-13), P1(13-23)
Turnaround times:

- P1: 23 - 0 = 23
- P2: 5 - 1 = 4
- P3: 13 - 2 = 11

Waiting times:

- P1: (0-0) + (13-1) = 12
- P2: 0
- P3: 5 - 2 = 3

Average waiting time: $(12 + 0 + 3)/3 = 5$

Problem 2: Network Design

(a) Network types:

- Main office: LAN (Ethernet)
- Branch connection: WAN (VPN over Internet or leased line)
- Mobile workers: PAN for local, mobile data or Wi-Fi for connectivity

(b) Networking devices:

- Main office: Switch(es), Router, Firewall, Wireless Access Point
- Branch office: Router, Switch, possibly firewall
- Connection: Router with VPN capability at both ends

(c) Addressing:

- Private IP addresses (e.g., 192.168.x.x)
- DHCP for automatic addressing
- VLANs for segmentation (e.g., departments, guests)
- NAT for Internet access

Problem 3: Component Selection

(a) Voltage regulation: Voltage regulator IC (e.g., 7805) or switching regulator

(b) Signal amplification: Operational amplifier or transistor amplifier circuit

(c) Energy storage: Capacitor (short term) or battery (long term)

(d) AC to DC: Rectifier circuit with diodes and filter capacitor

(e) Overvoltage protection: Zener diode or TVS (Transient Voltage Suppressor)

(f) Wireless communication: Bluetooth module, Wi-Fi module, or RF transceiver

7.3 Exam 3 Solutions

Problem 1: Transistor Amplifier

Design specifications: $A_v \geq 50$, $Z_{in} \geq 1k\Omega$, $\beta = 200$

(a) Voltage gain $A_v \approx R_C/R_E$ (for bypassed R_E) To get $A_v = 50$, choose $R_C = 5k\Omega$, $R_E = 100\Omega$ But $Z_{in} \approx \beta R_E = 200 \times 100 = 20k\Omega > 1k\Omega$

(b) DC biasing: $V_E \approx I_E R_E$, choose $I_C \approx I_E = 1mA$ $V_E = 1mA \times 100\Omega = 0.1V$ $V_B = V_E + 0.7 = 0.8V$ $V_C = V_{CC} - I_C R_C = 12 - 5 = 7V$

Base current $I_B = I_C/\beta = 1mA/200 = 5\mu A$

Choose R_2 such that $I_{divider} \approx 10 I_B = 50\mu A$ $R_2 = V_B/50\mu A = 0.8/50\mu = 16k\Omega$

$R_1 = (V_{CC} - V_B)/51\mu A \approx 11.2/51\mu = 220k\Omega$

(c) Coupling capacitors: $f_{low} = 100Hz$, choose C such that $X_C = R/10$ at f_{low} For input: $R = Z_{in} \parallel R_1 \parallel R_2 \approx 1k\Omega$ $C_{in} = 1/(2\pi f R/10) = 1/(2\pi \times 100 \times 100) = 15.9\mu F$, use $22\mu F$

For output: $R = R_C \parallel R_L$ (assume $R_L = 10k\Omega$) $R_{out} = 5k \parallel 10k = 3.33k\Omega$ $C_{out} = 1/(2\pi \times 100 \times 333) = 4.8\mu F$, use $10\mu F$

Problem 2: Digital System

(a) Maximum data rate: 8-bit data, 50 MHz clock If each transfer takes 1 cycle: $50 \times 10^6 \times 8 = 400$ Mbps If DDR: 800 Mbps

(b) MIPS calculation: Clock = 50 MHz, CPI = 4 cycles/instruction Instructions/second = $50 \times 10^6/4 = 12.5 \times 10^6$ IPS = 12.5 MIPS

(c) Address decoding for 64 KB: 16-bit address bus: $2^{16} = 64K$ addresses 64 KB memory requires all 16 address lines No decoding needed if using entire space If using multiple devices: Use higher address bits for chip select

Problem 3: Integrated Design

(a) Signal conditioning:

- Sensor: 0-5V for 0-100řC
- Microcontroller: 3.3V ADC reference
- Need voltage divider: $5V \rightarrow 3.3V$, ratio = 3.3/5 = 0.66
- Use resistors: 3.3k and 1.7k (or 33k and 17k)

(b) Resolution: 10-bit ADC: $2^{10} = 1024$ steps Temperature range: 100řC Resolution = $100/1024 \approx 0.098C$ per step

(c) Flowchart:

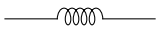
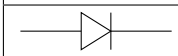
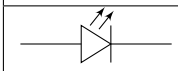
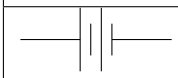
(a) Start
(b) Initialize system
(c) Read ADC value
(d) Convert to temperature: $T = (ADC/1024) \times 100$
(e) Display temperature on LCD
(f) If $T > 80C$: Activate buzzer
(g) Delay (e.g., 1 second)
(h) Repeat from step 3

Appendices

Electrical Units and Prefixes

Prefix	Symbol	Factor	Example
Tera	T	10^{12}	THz (Terahertz)
Giga	G	10^{9}	GHz (Gigahertz)
Mega	M	10^{6}	MHz (Megahertz)
kilo	k	10^{3}	k (kilohm)
-	-	10^{0}	Hz (Hertz)
milli	m	10^{-3}	mA (milliampere)
micro		10^{-6}	F (microfarad)
nano	n	10^{-9}	ns (nanosecond)
pico	p	10^{-12}	pF (picofarad)

Basic Electrical Components

Symbol	Component	Name
	Resistor	Resistor
	Capacitor	Capacitor
	Inductor	Inductor
	Diode	Diode
	LED	Light Emitting Diode
	Battery	Battery
	NPN Transistor	NPN Transistor
	PNP Transistor	PNP Transistor

Useful Formulas

- Ohm's Law: $V = IR$
- Power: $P = VI = I^2R = V^2/R$
- Resistors in series: $R_{total} = R_1 + R_2 + \cdots + R_n$
- Resistors in parallel: $\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n}$

- Capacitors in series: $\frac{1}{C_{total}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n}$
- Capacitors in parallel: $C_{total} = C_1 + C_2 + \cdots + C_n$
- Time constant (RC): $\tau = RC$
- Frequency/Period: $f = 1/T$, $T = 1/f$
- Angular frequency: $\omega = 2\pi f$

Appendix E: Color Code for Resistors

Color	Digit	Multiplier	Tolerance	Temp Coeff.
Black	0	10^0	-	250 ppm/K
Brown	1	10^1	ś1%	100 ppm/K
Red	2	10^2	ś2%	50 ppm/K
Orange	3	10^3	-	15 ppm/K
Yellow	4	10^4	-	25 ppm/K
Green	5	10^5	ś0.5%	20 ppm/K
Blue	6	10^6	ś0.25%	10 ppm/K
Violet	7	10^7	ś0.1%	5 ppm/K
Gray	8	10^8	ś0.05%	1 ppm/K
White	9	10^9	-	-
Gold	-	10^{-1}	ś5%	-
Silver	-	10^{-2}	ś10%	-

References and Resources

Online Resources

- All About Circuits: https://www.allaboutcircuits.com
- Khan Academy - Electrical Engineering: https://www.khanacademy.org/science/electrical-engineering
- MIT OpenCourseWare - Circuits and Electronics: https://ocw.mit.edu/courses
- CircuitLab: Online circuit simulator
- Falstad Circuit Simulator: Interactive circuit simulations

Software Tools

- **LTspice** – Free SPICE simulator from Analog Devices for electronic circuit analysis.
- **Proteus** – Electronics design and simulation software with microcontroller support (Arduino, PIC, etc.).
- **Multisim** – Professional simulation for analog and digital electronic circuits.
- **PSpice** – Industry-grade electronic circuit simulator.
- **TINA-TI** – Circuit simulation software from Texas Instruments.
- **Fritzing** – PCB design and electronic prototyping tool.
- **KiCad** – Open-source professional PCB design software.
- **EasyEDA** – Online PCB design and simulation platform.
- **MATLAB / Simulink** – Modeling and simulation of electrical and control systems.
- **PSIM** – Simulation software for power electronics (inverters, converters, rectifiers).
- **Arduino IDE** – Development and simulation environment for Arduino microcontrollers.

Final Word

This workbook was created to help students understand Electronics and system components in a clear and practical way. It explains the main ideas and includes examples and exercises to make learning easier.

Special thanks to Dr.**MENASSEL Rafik & Dr.Tarek Nouioua** for providing the original course material and guidance. His support made it possible to prepare this workbook and adapt it to help students learn more effectively.

Abdeljalil Mostefaoui

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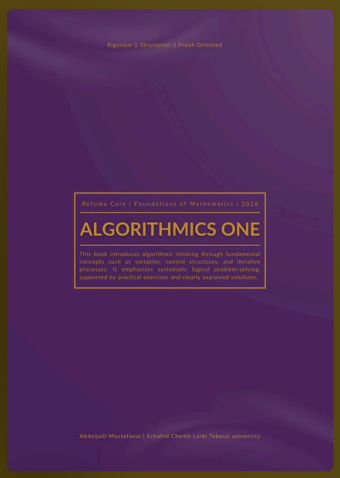
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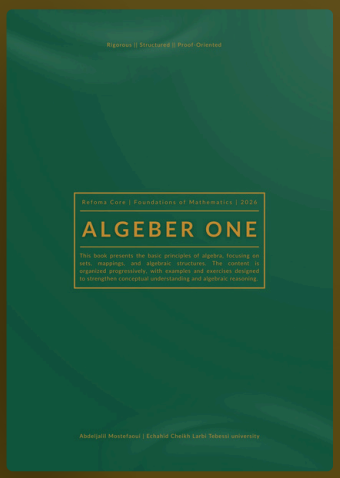
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